AMENDMENTS TO THE SPECIFICATION:

Please amend paragraph 0019, beginning on page 4, as follows:

[0019] Figs. 1A and 1B show a basic electrical schematic 10 of circuitry to implement over-dwell and blinding timer functions and exemplary waveforms illustrating functional operation of the circuitry, respectively. During normal operation, when an electronic spark timing (EST) signal voltage rises, a coil current switching device is turned on and coil charging begins with activation of the coil current switching device. Simultaneously therewith, a logic signal, i.e., an inverted version of the EST signal, turns off transistor ~~10~~ 11. When the transistor ~~10~~ 11 is turned on, timing capacitor C1 is shorted and, as such, is in a discharged state. When the transistor ~~10~~ 11 is turned off, the capacitor C1 begins charging via current delivered by resistor R1, which is coupled between a battery at a voltage B+ and the capacitor C1. The charging current continues (for a time TOREF1) until the voltage across the capacitor C1 reaches a voltage level defined by a reference voltage Vref applied to an inverting input of comparator 12.

Please amend paragraph 0021, beginning on page 5, as follows:

[0021] With an understanding of the basic timer functions, it should be appreciated that currents into or out of the non-inverting input of the comparator 12, the transistor ~~10~~ 11, or the discharge current source 16 (during the charging period) affect the over-dwell time. In order to prevent significant modification of the over-dwell time, it is generally desirable that these currents not have a net total exceeding more than a few tens of nanoamps. According to one embodiment of the present invention, a comparator circuit constructed according to the present invention provides a substantial reduction in input currents while preserving the accuracy of the comparator function. Additionally, a blinding timer function may be included that is designed to limit the amount of leakage current attributable to the discharge current source coupled to the timing capacitor node.

Please amend paragraph 0036, beginning on page 11, as follows:

[0036] With reference to Fig. 6, a transistor level schematic 100 of one embodiment of the present invention is shown. Transistors QT6 and QT9 form a basic emitter-coupled transistor pair of a comparator. Timing capacitor C1 and timing resistor R1 are connected at node "Vin" at the base of transistor QT2. This is the node of interest for maintaining minimal current perturbation. Diode connected transistors QT3 and QT10 are represented by diodes D1 and D2 in Fig. 3. Transistors QT7 and QT17 form the current source I3 (Fig. 3) and transistors QT12 and QT18 form the current source I1. The current source I4 (see Fig. 3) is composed of transistors QT19 and QT21. Transistor QT13 of Fig. 6 corresponds to the transistor Q7, of Fig. 3, and resistor RT2 corresponds to the resistor R10 of Fig. 3.

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